REMARKS

This Reply is being filed in response to the Office Action dated June 6, 2006. This amendment is accompanied by a Request for a One-Month Extension of Time and the appropriate fee for the Extension of Time. At the time of the Office Action, claims 1-13 were pending in the application. All pending claims have been rejected under the judicially created doctrine of obviousness-type double patenting. Claims 1-3 have been rejected under 35 USC §103(a). Claim 1 has been amended for greater clarity and to provide proper antecedent basis. Claim 13 has been amended to correct a typographical error. The rejections are set out in more detail below.

I. Double Patenting

Claims 1-13 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-27 of U.S. Patent No. 6,770,159 to Tebbe, et al. ("Tebbe et al. '159"). Applicants appreciate Examiner noting that a timely filed terminal disclaimer in compliance with 37 CFR §1.321(c) may be used to overcome a rejection based on a non-statutory double patenting ground based upon a commonly owned conflicting application or patent. Since the instant application and the Tebbe et al. '159 patent is commonly owned, a terminal disclaimer in accordance with 37 CFR §1.321(c) is enclosed to overcome the foregoing rejections. Please charge the fee associated with the filing of a terminal disclaimer pursuant to Fee Code 1814 to Deposit Account No. 08-0870. Accordingly, withdrawal of the double patenting rejection is respectfully requested.

II. Brief Review of Applicants' Invention

Prior to addressing the Examiner's rejections on the art, a brief review of applicants' invention is appropriate. The invention relates to a method for fabricating a textured dielectric substrate for an RF circuit. A textured substrate is a substrate having a geometric pattern of distinct areas formed within it. The method includes the step of selecting at least a first and a second dielectric substrate material. Each dielectric substrate material has at least one electrical property that is distinct from another

dielectric substrate. The first and second dielectric substrates are cut into a selected size and shape, forming a plurality of dielectric pieces. The dielectric pieces are then selectively arranged on a base plate to produce a textured substrate. The individual dielectric pieces can adhere to the base plate by disposing an adhesive layer between the dielectric pieces and the base plate and then allowing the adhesive layer to cure. The textured substrate that is produced has at least one effective electrical property at a frequency of interest that is different from a bulk electrical property of each individual one of the dielectric board material at the frequency of interest.

II. Claim Rejections on Art based on §103(a)

Claims 1-3 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,036,798 to Nishide, et al. ("Nishide et al."), in view of Tebbe et al. '159. Significantly, the invention disclosed in the Tebbe et al. '159 qualifies as prior art only under 35 U.S.C. §102(e). The invention is described in a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent. See 35 U.S.C. §102(e)(2). Therefore, Examiner's attention is directed to 35 U.S.C. §103(c)(1). That statutory section provides that:

> Subject matter developed by another person, which qualifies as prior art only under one or more subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.
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> 35 U.S.C. §103(c)(1)

Applicants wish to inform the Examiner that the present application and U.S. Patent No. 6,770,159 are commonly assigned to Harris Corporation of Melbourne, Florida. Copies of the recorded assignment documentation are enclosed herewith for the Examiner's convenience. In view of the foregoing, Applicants respectfully submit that the combination of Tebbe et al. '159 and Nishide et al. cannot be properly used as the basis for forming an obviousness rejection under 35 U.S.C. §103.

Claims 1-3 have also been rejected under 35 U.S.C. §103(a) as being unpatentable over Nishide, et al. ("Nishide et al."), in view of JP 09260105 ("'105"). Nishide et al. teaches a process for producing an electronic part, such as an RF circuit. The process is comprised of the step of separately firing at least two substrates having different electrical characteristics (Nishide et al., Col. 1, lines 65-67). Each of these substrates contains therein a passive element (Nishide et al., Col. 1 line 67 – Col. 2, line 1). Notably, the individual substrate layers are stacked one on top of the other, forming a multi-layer structure (Nishide et al., Fig. 1; Col. 2, lines 46-58). The individual substrate layers adhere to each other using an adhesive 3, forming a laminate (Fig. 1; Col. 3, lines 16-17). Further, each passive element within each substrate is electrically connected to an outer electrode 4 located on the surface of the laminate of substrates (Fig. 1, Col. 4, lines 10-13).

The '105 reference discloses a chip mold thermistor assembly and its method of manufacture. The method includes disposing surface electrodes 2, 3 on the top and bottom surfaces of a ceramic wafer 1 (See Fig. 1(c)). The ceramic wafer 1 is then cut in a grid-like fashion (marked by arrows C1 and C2 in Fig. 1(c)) into multiple thermistor elements 4 (See Fig. 1(e)). An adhesive agent 8 is coated on the surface of an alumina board 5 (See Figs. 1(f) and (g)). The top surface of the alumina board 5 (as shown in Fig. 1(f)) contains grid-like markings 6, 7 that delineate the location(s) for placing and adhering the thermistor elements 4 onto the alumina board 5. Once a resin is applied to the alumina board, the alumina board is co-fired along with its adhered-to thermistor elements. The alumina board hardens from the co-firing process and is then cut into rectangular plates along an axis marked by arrows C3 (See Figs. 2 and 3). Each rectangular plate is coated along its elongated length with a silver paste, which is allowed to dry and harden, forming a terminal electrode 14 on either side of the joined thermistor element assemblies 4 (See Figs. 4 and 5). Finally, the rectangular plate is cut along an axis marked by arrows C4 (See Fig. 4), forming separate individual chip-type thermistor assemblies 4. Each separate thermistor assembly is bonded to an underlying ceramic piece.

Applicants' amended independent claim 1 recites cutting each of the first and second dielectric board materials into a selected size and shape to form a plurality of dielectric pieces. In addition, amended claim 1 recites the step of selectively arranging each of a plurality of the dielectric pieces from the first and second dielectric board materials on a base plate in a pattern to produce a textured substrate having at least one effective electrical property at a frequency of interest that is different from a bulk electrical property of each individual one of the first and second dielectric board materials at the frequency of interest. Nishide et al. fails to teach or suggest either one of these steps. In Nishide et al., the different substrates are not each arranged on a base plate. Rather, the substrates in Nishide et al. are stacked one on top of the other (please refer to Figs. 1 and 2 of Nishide et al.).

The above distinction is important. In Nishide et al. the motivation for stacking independently pre-fired substrate layers is towards improving the process of manufacturing electronic parts with laminated substrates. The Nishide et al. process reduces the potential for warpage or cracks of the substrates (Nishide et al. Col. 1, lines 57-61). In contrast, Applicants' invention seeks to improve the flexibility in designing a RF circuit by improving the choice of electrical properties available. Moreover, Applicants' invention allows RF circuit designers to selectively change the electrical properties of a substrate in the implementation of a particular RF circuit design by combining different substrate pieces to form a larger textured substrate. The net effect is a blending of the various electrical characteristics, which facilitates the tailoring of the overall electrical properties of the newly formed textured substrate (Applicants' Specification, ¶16).

Similarly, the '105 reference fails to make up for the deficiencies present in Nishide et al. In the '105 reference, there is no selective arrangement of different dielectric pieces. Instead, the '105 reference teaches away the idea of arranging dielectric pieces having different electrical properties. In the '105 reference, the goal is to improve the mass-production of individual chip type thermistors. The thermistor assemblies are formed on a presumably pre-manufactured wafer having one set of electrical characteristics ('105, Fig. 1(a)). The wafer is then cut up/divided into identical thermistor components. In contrast, Applicants' invention takes various different

substrate pieces having different electrical properties and selectively arranges them on a base plate surface. The result of this selective arrangement is a larger and seemingly continuous substrate layer. This is done to improve the flexibility of circuit design, a point that is unaddressed by either Nishide et al. or the '105 reference. None of these references is concerned or make mention of tailoring the overall electrical characteristics of a textured substrate.

In view of the foregoing, Applicants believe that Nishide et al., the '105 reference, and/or their combination fail to teach, suggest or motivate one of ordinary skill in the art to practice the combination proposed by the Examiner. Thus, a rejection under §103(a) is not justified. Accordingly, Applicants believe claim 1 as amended is in a condition for allowance and the rejection under 35 U.S.C. §103(a) must be withdrawn. Moreover, Applicants believe claims 2-13 are allowable at least by virtue of their dependency on an allowable base claim.

The Commissioner is hereby authorized to charge any fees which may be due by submission of this document to Deposit Account No. 08-0870.

Respectfully submitted,

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Date

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